UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,074	04/19/2001	Mark A. Maciver	GB900051US1	9566

46369 7590 12/03/2004

HESLIN ROTHENBERG FARLEY & MESITI P.C.
5 COLUMBIA CIRCLE
ALBANY, NY 12203

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,074	MACIVER, MARK A.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1-12 and newly added claims 13-18 filed June 24, 2004 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Byers (prior art of record) does not teach error correction." The Examiner respectfully disagrees. Byers teaches that a key design element of high reliability computer systems is that of *error detection and correction*. It has long been recognized that the integrity of the data bits within the computer system is critical to ensure the accuracy of operations performed in the data processing system. The alteration of a single data bit in a data word can dramatically affect arithmetic calculations or can change the meaning of a data word as interpreted by other sub-systems within the computer system. Byers teaches an error detection logic block 874 may be coupled to address input register 864 via interface 868. Error detection logic block 874 may comprise a SRAM address register 872. SRAM address register 872 may capture an SRAM address when an SRAM read error is detected. That is, SRAM address register 872 may store the read address that is present on DSD address bus 650 in response to an SRAM read error. Error detection block 874 may monitor the data that is present in DSD bus 650 via interface 754. Error detection block 874 may thus perform a parity check or the like on the data presently read from memory 680. If an error exists, error detection block 874 may enable SRAM address register thereby capturing the current read address. This may identify the faulty read address within memory 680. *Error correction block 874* may then

provide the faulty read address to USBC0 640 for further processing via interface 820. For example, USBC0 640 may read and write various test patterns to the faulty read address to determine if the fault was caused by a soft error or a hard error. If the fault was caused by a soft error, the contents of memory 680 may be reloaded and the operation of the computer system may continue. However, if the fault was caused by a hard error, the operation of the computer system may be interrupted. Other error detection schemes are contemplated and may be incorporated into error detection block 874. Byers teaches (Figure 9) a table illustrating an exemplary bus description of the DSD bus of FIG. 7. The table is generally shown at 900. DSD bus 650 may comprise a number of fields. The type of fields can be generally broken down into data fields, address fields, parity fields, and control fields. The fields for an exemplary embodiment of DSD bus 650 are described below. DSD bus 650 may comprise a 32 bit data bus as shown at 902. The 32 bit data bus is a bi-directional data bus and may serve as the main data path for all operations. The 32 bit data bus may be asserted by a bus master for write operations and a bus slave for read operations. DSD bus 650 may further comprise a 4 bit data parity bus as shown at 904. Each of the four parity bits may correspond to predetermined data bits of 32 bit data bus 902. The *4 bit data parity bus may be used for error detection and correction purposes.* Furthermore, the Examiner would like to comment on the Applicant's contention the there is a typographical error within the disclosure of Byers. It is well known in the art that error detection and correction processes are usually done together. There would be any point in detecting an error if you weren't going to correct it. Although, most of Byers's patent is concerned with error detection, error correction is contemplated and taught. Therefore

for the purposes of limitations stated in the claims of the present application, the rejection is appropriate and valid.

Applicant contends, "...there is absolutely no teaching in Byers of how to correct an error." The Examiner respectfully disagrees. Byers teaches as stated above error correction. Furthermore, the Examiner would like to point out that independent claim 1 of the present application only states to detect and correct and error, not how to correct it. See claim 1, lines 9-10.

Applicant contends, "...Byers does not teach error correction in the second portion..." The Examiner respectfully disagrees. Byers teaches (col. 4, lines 9-68) a central hardware element which may validate all bus transmissions, regardless of which user has a fault detection capability provided therein. That is, the transceivers of a selected one of the users may monitor all data transmissions on the bus, and check the parity thereof. Any transmission between any two or more users, including the selected one of the users, may be validated by the central hardware element. This may allow the exemplary embodiment to check the parity of otherwise un-checked data transmissions over the bus. It is contemplated that the central hardware element may be located in at least one of the users or may be provided in a separate element which is coupled to the bus. If the central hardware element is provided in a separate element which is coupled to the bus, the transceiver may comprise only an input buffer. The input buffer being necessary to monitor the bus transmissions. Finally, it is contemplated that the input buffers of a user may provide the value of the data word on the bus to the user such that a parity check may be performed by the user, regardless of whether the corresponding user is a transmitting user, a receiving user, or neither. The centralization of the error detection function

helps to isolate where an error actually occurred. That is, since all bus transmission may be monitored regardless of which user is the transmitting user or the receiving user, the exemplary embodiment may determine which transmission provided the error therein. For the memory read/write example described above, the exemplary embodiment may check the parity of a data write transmission to a memory and a corresponding data read transmission from the memory.

Applicant contends, "...Applicant recites detecting and correcting multiple errors ...in contrast to Byers which can only detect and correct one error at a time." The Examiner respectfully disagrees and quotes Applicant's admission that Byers teaches to detect and correct one error at a time. The Examiner would like to point out that Byers teaches (col. 1, lines 60-68) a single parity bit in conjunction with a multiple bit data word can detect a single bit error within the data word. However, it is also readily known that a single parity bit in conjunction with a multiple bit data word can be defeated by multiple errors within the data word. As calculation rates increase, circuit sizes decrease, and voltage levels of internal signals decrease, the likelihood of a multiple errors within a data word increase. Therefore, methods to detect multiple errors within a data word are essential. In response thereto, system designers have developed methods for detecting multiple errors within multiple bit data words by providing multiple parity bits for each multiple bit data word.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. (USPN 5784393).

As per claims 1, 7 and 13, Byers et al. (herein after: Byers) substantially teaches (title and abstract) a method and apparatus for providing fault detection to a corresponding bus when one or more of the users connected to the bus does not have a fault detection capability provided therein. Furthermore, Byers teaches a method and apparatus for performing fault detection on a corresponding bus when the width of the bus is insufficient to accommodate a number of parity bits. In an exemplary embodiment, a selected one of the number of users may validate all bus transmissions via a number of transceivers, regardless of which user has a fault detection capability provided therein. In another exemplary embodiment of the present invention, a transmitting user may provide a data word and a number of corresponding parity bits. The transmitting user may provide the data word to the bus while storing the corresponding number of parity bits therein. The data word may be provided back to the transmitting user via the corresponding transceivers wherein the transmitting user may check the data word against the number of parity bits previously generated by the transmitting user. In particular, Byers teaches (Figure 3) a first portion and a second portion of a data processing system that transmits a data word with corresponding parity bits. In the second portion Byres teaches to test and detect errors in the received information via the parity checker.

Byers does not explicitly teach a parity generator in the first portion as stated in the present application.

However, Byers teaches (col. 1, lines 44-59) that typical system which uses parity as an error detection mechanism has a *parity generation circuit* for generating the parity bit. For example, when the system stores a data word into a memory, the parity generation circuit generates a parity bit from the data word and the system stores both the data word and the corresponding parity bit into an address location in the memory. When the system reads the address location where the data word is stored, both the data word and the corresponding parity bit are read from the memory. The parity generation circuit then regenerates the parity bit from the data bits read from the memory device and compares the regenerated parity bit with the parity bit that is stored in memory. If the regenerated parity bit and the original parity bit do not compare, an error is detected and the system is notified. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a parity generator at the first portion of the data processing system as stated in the present application. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that a parity generator is essential in generating parity and it would have been convenient for a designer to place at the first portion of the data processing system.

As per claims 2, 8 and 15, Byers substantially teaches, in view of above rejection, a connector as stated in the present application. The Examiner would like to point out that for all practical purposes an interface is a connector. An interface is defined as *a surface forming a common boundary between adjacent regions, bodies, substances, or phases.* A connector is defined as *something that joins or links together.* Furthermore, Byers teaches (abstract) a method

and apparatus for providing fault detection to a corresponding bus when one or more of the users are **connected** to the bus.

As per claims 3, 7 and 14, Byers substantially teaches, in view of above rejection, (Figure 6) is a schematic diagram of an exemplary embodiment of the host interface adapter block. For illustration, Host Interface Adapter (HIA) 534 of FIG. 5 is shown. It is recognized that HIA 544 may be similarly constructed. HIA 534 may comprise two Microsequencer Bus Controllers (USBC) 640, 642 which may be connected to a control store 644 via interface 646. The USBC's 640, 642 may access the HIA stations 628, 622, 618, and 636 via a microbus 638. A player+0 602 and a player+1 600 may receive frames (or data elements) over fiber optic link 530. The term player+ refers to a fiber optic interface controller available from National Semiconductor which is called the Player Plus Chip Set. Player+0 602 may forward its frame to light pipe control 604 via interface 606. Similarly, player+1 600 may forward its frame to light pipe control 604 via interface 606. Light pipe control 604 may transfer the frames to a Receive Frame Transfer Facility (REC FXFA) 608 via interface 610. REC FXFA 608 may unpack the frames and may store control information in a Request Status Control Table-0 (RSCT-0) 628 and a RSCT-1 622 via interface 620. RSCT-0 628 and RSCT-1 622 may monitor the data that has been received from a corresponding data mover. The data which was contained in the frame received by REC FXFA 608 may be sent to the Database Interface (DBIF) station 618 via interface 620. DBIF 618 may forward the data over interface 632 to the streets.

As per claims 4-6, 10-12 and 16-18, Byers substantially teaches, in view of above rejection, (col. 22, lines 1-25) an error detection logic block 874 may be coupled to address input register 864 via interface 868. Error detection logic block 874 may comprise a SRAM address

register 872. SRAM address register 872 may capture an SRAM address when an SRAM read error is detected. That is, SRAM address register 872 may store the read address that is present on DSD address bus 650 in response to an SRAM read error. Error detection block 874 may monitor the data that is present in DSD bus 650 via interface 754. Error detection block 874 may thus perform a parity check or the like on the data presently read from memory 680. If an error exists, error detection block 874 may enable SRAM address register thereby capturing the current read address. This may identify the faulty read address within memory 680. Error correction block 874 may then provide the faulty read address to USBC0 640 for further processing via interface 820. For example, USBC0 640 may read and write various test patterns to the faulty read address to determine if the fault was caused by a soft error or a hard error. If the fault was caused by a soft error, the contents of memory 680 may be reloaded and the operation of the computer system may continue. However, if the fault was caused by a hard error, the operation of the computer system may be interrupted. Other error detection schemes are contemplated and may be incorporated into error detection block 874.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claims 1-12 and newly added claims 13-18. All arguments have been considered. It is the Examiner's conclusion that amended claims 1-12 and newly added claims 13-18 are not patentably distinct or non-obvious over the prior art of record. See office action above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
November 17, 2004

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100